REMARKS

Claims 1-4 and 6-15 are now present in this application.

The abstract and claims 1, 10 and 13 have been amended, and claim 5 has been cancelled without prejudice or disclaimer of the subject matter contained therein. Reconsideration of the application, as amended, is respectfully requested.

Objection to the Abstract

The Abstract stands objected to for certain informalities. In view of the foregoing amendments, it is respectfully submitted that this objection has been addressed. Reconsideration and withdrawal of any objection to the abstract are respectfully requested.

Rejection under 35 USC 112

Claim 5 stands rejected under 35 USC 112, first paragraph. This rejection is respectfully traversed.

Without conceding the appropriateness of the Examiner's rejection, but simply to expedite prosecution, it is noted that this claim 5 has been cancelled, thereby rendered this rejection moot.

Rejection under 35 USC 102(b)

Claims 1-4, 6-8 and 10-12 stand rejected under 35 USC 102(b) as being anticipated by Vinekar, U.S. Patent 5,518,310. This rejection is respectfully traversed.

With regard to claim 1, Vinekar describes a method of storing an array of digital data into a memory having a plurality of memory pages, each memory page having a first memory section and a second memory section, the method comprising the steps of dividing the array of digital data into a plurality of block units, each of the block units having a plurality of odd rows and a plurality of even rows, each of the odd rows and the even rows having at least one byte (see col. 9, lines 52-56); storing subsequent odd rows of at least one of the block units into consecutive storage locations in the first memory section, and storing subsequent even rows of at least one of the block units into consecutive storage locations in the second memory section (see col. 12, line 46 - col. 13, line 11, and Figs. 8 and 9).

Col. 12, lines 46-51, and Figs. 8 and 9 of Vinekar, state that, "As depicted in tables 800 and 900 in FIGS. 8 and 9, respectively, the odd and even field portions of both halves of the image macroblocks are written into **different** odd and even buffer pages within video frame store memory 80 (see FIG. 1), with appropriate 4-byte positional offsets as taught by our invention." Hence, in Vinekar, the data of odd field of **each** image macroblock are written into **different** odd buffer pages. For example, the odd data of half 720 of Macroblock M1 (710) in Figure 7 are written into Page 0 (Bank 0), shown in Figure 8, and the odd data of half 730 of Macroblock M1 (710) are written into Page 1 (Bank 1), shown in Figure 9.

Alternately, in claim 1 of the present invention, subsequent odd rows of at least one of the block units are written into consecutive storage locations in the first memory section, and subsequent even rows of at least one of the block units into consecutive storage locations in the second memory section. In other words, subsequent odd rows of at least one of the block units are written into **same** buffer page (consecutive storage locations in the first memory section).

In addition, Vinekar does not teach one that "subsequent odd rows of at least one of the block units are wrote into **same** buffer page".

Accordingly, it is respectfully submitted that the method of independent claims 1 and 10, as well as their dependent claims, is neither taught nor suggested by the prior art utilized by the Examiner. Reconsideration and withdrawal of the 35 USC 102(b) rejection are respectfully requested.

Rejection under 35 USC 103

Claims 9 and 13-15 stand rejected under 35 USC 103 as being unpatentable over Vinekar in view of McGuinness, U.S. Patent 6,104,416. This rejection is respectfully traversed.

With regard to claim 9, Vinekar is relied upon for the teachings as discussed above relative to claim 8.

However, Vinekar does not teach that m is equal to thirty-two. However, McGuinness describes a method of storing an array of digital data into a memory, the memory having a plurality of memory tiles, each memory tile having a first memory section (532, Figure 8) and a second memory section (534), the method comprising the steps of dividing the array of digital data into a plurality of block units, each of the block units having a plurality of odd rows and a plurality of even rows, storing subsequent odd rows of at least one of the block units into storage locations in the first memory section, and storing subsequent even rows of at least one of the block units into storage locations in the second memory section (see col. 11, line 51 - col. 12, line 13); wherein each of the block units has thirty-two rows (see col. 10, lines 43-53).

However, in Vinekar, the data of odd field of **each** image macroblock are written into **different** odd buffer pages. Alternately, in the present invention subsequent, odd rows of at least one of the block units are written into **same** buffer page. Therefore, it would not have been obvious to one of ordinary skill in the art at the time the present invention was made to modify the device of Vinekar so that m is equal to thirty-two as suggested by McGuinness.

With regard to claim 13, in Vinekar, the data of odd field of **each** image macroblock are written into **different** odd buffer pages. Alternately, in the present invention subsequent, odd rows of at least one of the block units are written into **same** buffer page. Therefore, it would not have been obvious to one of ordinary skill in the art at the time the present invention was made to modify the device of Vinekar to include retrieving a prediction block of picture from the memory, retrieving the digital data representing the prediction block stored in the first memory section, and retrieving the digital data representing the prediction block stored in the second memory section as suggested by McGuinness.

Accordingly, it is respectfully submitted that the method of 9 and 13-15 is neither taught nor suggested by the prior art utilized by the Examiner. Reconsideration and withdrawal of the 35 USC 103 rejection are respectfully requested.

Conclusion

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

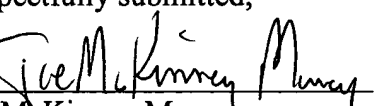
In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), the Applicants respectfully petition for a two (2) month extension of time for filing a response in connection with the present application and the required fee of $450.00 is attached herewith.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: August 22, 2005

Respectfully submitted,

By 

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